Phase Detector

CD-552R3 CD-552R4

CD-552R series detectors are an on-board phase detectors possessing frequencies falling within the range of 1kHz to 200kHz for CD-552R3 and frequencies falling within the range of 10kHz to 2MHz for CD-552R4.
The signal system is composed of the phase sensitive detector (PSD), low-pass filter (LPF), and output amplifier. A low-pass expansion of output low-pass filter cut-off frequency is available with the addition of one external resistor, and the gain setting (×1 to ×10) is also enabled. The reference signal system consists of a 0°-90° phase shifter (PAT.P) and 50%-duty circuit (PAT.P), which enables the detection of A sin ϕ or A cos ϕ phase. The phase detection with double frequency is permitted if 2f mode is placed through the connection with the specified pin.
CD-552R series detectors are in a static-shielded 20-pin single inline package.

▼Absolute maximum ratings

Supply voltage (±Vs)	±18V
Signal input voltage	±Vs
Reference signal input voltage	+5.5V, –0.5V
Logic control voltage	+5.5V, –0.5V

▼Signal system

▽**Signal input**

Model	**CD-552R3**	**CD-552R4**
Input impedance	Max. 10kΩ ±5% at 1kHz	Max. 2.5kΩ ±5% at 10kHz
Linear maximum input voltage	Min. ±10V	
Allowable slew rate	Max. 5V/μs	Max. 130V/μs

▽**Phase detector**

Detection method	Synchronous rectifying type by square-wave multiplication	
Detection characteristics	Vout=Vin • A • cosϕ Vout: Detection DC output Vin: Input signal (synchronization) A: Gain ϕ: Phase difference between the signal system and reference signal system	
Operating frequency range	1kHz to 200kHz	10kHz to 2MHz
Gain (ϕ=0)	1Vdc/$V_{o\text{-}p}$(sine-wave): Pins ⑫ and ⑬ open 10Vdc/$V_{o\text{-}p}$(sine-wave): Short in Pins ⑫ and ⑬ Selectable in the 1 to 10-Vdc/Vo-p with the external resistor (Pins ⑫ and ⑬)	
Gain accuracy	±3%	
Phase difference (signal system and reference signal system)	–0.05° (typ) at 1kHz, –8° (typ) at 200kHz	–0.5° (typ) at 10kHz, +13° (typ) at 2MHz

▽**Low-pass filter**

Order	1-pole (6dB/oct)	
Cut-off frequency	Pins ⑨-⑩ shorted, Low-pass expansion is enabled with an external resistor or capacitor.	Pins ⑨-⑩ shorted, Low-pass expansion is enabled with an external resistor or capacitor.

▽**Detection output**

Output impedance	Max. 50Ω ±10% at 1kHz	Max. 50Ω ±10% at 10kHz
Linear maximum input voltage	±10V (DC, Load resistance≥2kΩ)	
Linear maximum input current	±5mA (DC)	
Offset voltage	±15mV, ±5mV (typ) Short in input, Gain: 1Vdc/Vo-p	
Offset voltage adjustment	Zero adjustment available with external pre-set resistors. (Pin ⑭)	

▼Reference signal system

▽**Reference signal input**

Model	**CD-552R3**	**CD-552R4**
Input circuit	CMOS Schmitt trigger, pulled up at 100 kΩ Trip point: +3.5V/+1.5V (typ)	
Input voltage	CMOS (0/+5V) level	
Unipolar (1f) mode	A rising or falling edge is regarded as a reference.	
Polarity switch	Pin ⑰ open or +5V: Rising edge regarded as a reference 0V: Falling edge regarded as a reference	
Pulse duration	Min. 50ns	
Bipolar (2f) mode	Both rising and falling edge are regarded as a reference.	
Mode setting	Connected with the reference signal input (Pin ⑱) and polarity switch input (Pin ⑰).	
Input waveform	Duty: 50%	
Input frequency range	1kHz to 100kHz	10kHz to 1MHz

▽**0°-90° phase shifter**

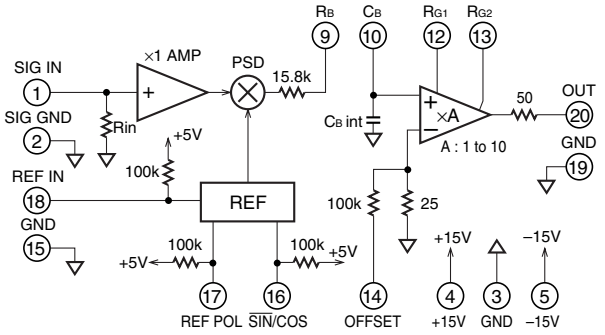
Function	This enables the detection of COS or SIN through a 0°-90° phase shift of reference signal input (Pin ⑱).
0°-90° phase difference	–90±0.5°, –90±0.1° (typ)
Control	Pin ⑯ open or +5V : 0° (COS) 0V : –90° (SIN)
Control input circuit	CMOS Schmitt trigger, pulled up at 100 kΩ

▼Others

Recommended supply voltage		±15V±1V	
Quiescent current		±25mA, ±20mA (typ)	±35mA, ±26mA (typ)
Temperature/ humidity range	**Operation**	–20°C to 70°C, 10 to 90%RH	
	Storage	–30°C to 80°C, 10 to 80%RH	
Dimensions		67×10.5×20mm (protrusion not included) Type SS20 (20-pin shielded SIP)	
Weight (NET)		Approx. 20g	

Note: The following specifications are applied unless otherwise specified:
23±5°C, Supply voltage: ±15V

Block diagram



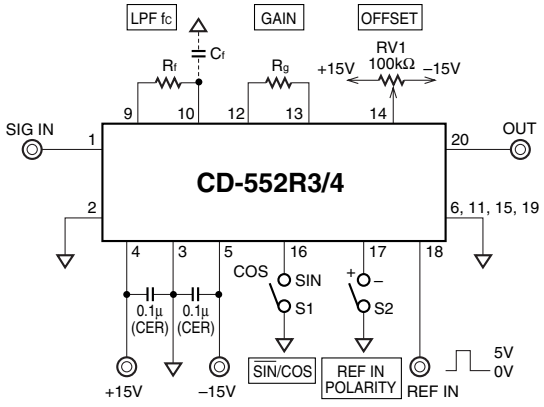
	CD-552R3	CD-552R4
Rin	10k	2.5k
CBint	10000p	1000p

SIN/COS This is used to switch the internal phase shifter between 0° and 90°, which enables the switching of detector input/output between A sin ϕ and A cos ϕ.
[A: Amplitude (o-p) of input signal, ϕ: Phase difference between input signal and reference signal]
HI: A•cosϕ (0°) (specified when the pin is open)
LO: A•sinϕ (90°)

REF POL This is used to switch the reference polarity of reference signals. An edge specified is a reference phase. With the REF POL terminal connected to the REF IN terminal, the phase detection with double frequency is enabled if 50% of duty is assigned to the reference signal.
HI: Rising edge regarded as a reference (specified when the pin is open)
LO: Falling edge regarded as a reference
Connected with REF IN terminal :
Both rising and falling edge regarded as a reference

OFFSET This is used to adjust output DC offset. ±15V is available for input, which allows both terminals of the pre-set resistor to be connected with ±15V input. The sliding terminal is connected to the OFFSET terminal. The signal is transmitted to the REF IN terminal with the SIG IN terminal connected to the ground, which brings the pre-set resistor into action to make offset adjustment.

Basic connection diagram



■*Gain setting*

CD-552R3/4 detectors are outfitted with the variable-gain output amplifiers (×1 to ×10). The maximum output voltage is set at 10Vo-p that should not be surpassed when setting proper gain for post processor.

$$Rg=\frac{2.9873\times10^{4}}{A-1}-3.3\times10^{3}[\Omega]$$

A: Gain [times (×)]

Example: Set points

Gain	×1	×2	×5	×10
Resistance	∞	26.7kΩ	4.12kΩ	0

■*LPF setting*

CD-552R3/4 detectors are outfitted with the primary LPF that is capable of setting frequencies of 1kHz (10kHz) or less with the use of the external CR. Proper frequency is to be allocated, allowing for the bandwidth, responsibility, and fluctuation for output signals.

CD-552R3

$$Rf=\frac{1}{2\pi\cdot(1\times10^{-8}+Cf\ [F])\cdot fc\ [Hz]}-15.9\times10^{3}\ [\Omega]$$

fc : Cut-off frequency
Cf : External capacitor

Example: Set points

Cut-off frequency (Equivalent noise bandwidth)	1Hz (1.57Hz)	10Hz (15.7Hz)	100Hz (157Hz)	1kHz (1.57kHz)
Resistance	1.43MΩ	1.58MΩ	143kΩ	0
Capacitance	0.1µF	–	–	–

R should remain at 2MΩ or less with the use of the eternal capacitor (Cf). Theory holds that a larger value can be assigned, but potential deterioration in offset, DC drift and noise may be concerned if assigned.

CD-552R4

$$Rf=\frac{1}{2\pi\cdot(1\times10^{-9}+Cf\ [F])\cdot fc\ [Hz]}-15.9\times10^{3}\ [\Omega]$$

fc : Cut-off frequency
Cf : External capacitor

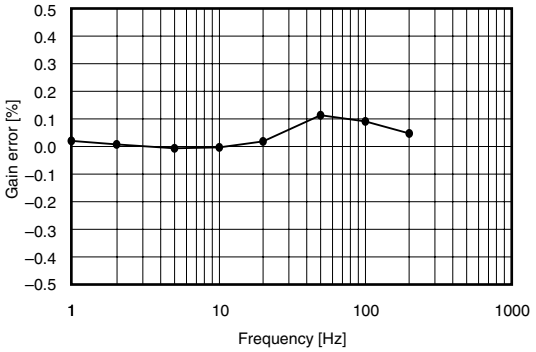
Example: Set points

Cut-off frequency (Equivalent noise bandwidth)	10Hz (15.7Hz)	100Hz (157Hz)	1kHz (1.57Hz)	10kHz (15.7kHz)
Resistance	140kΩ	1.58MΩ	143kΩ	0
Capacitance	0.1µF	–	–	–

Characteristics CD-552R3

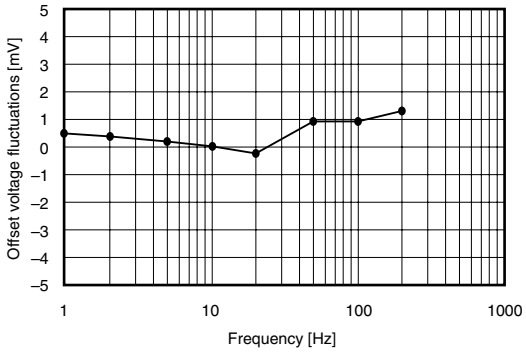
Gain fluctuations

Reference: 10kHz, Gain: ×10

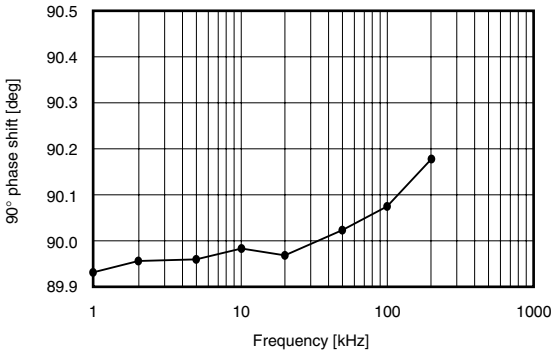


Offset voltage fluctuations

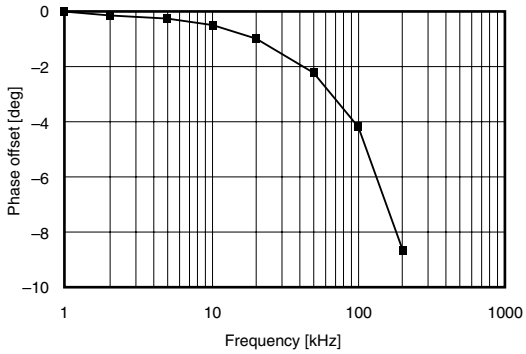
Reference: 10kHz, Gain: ×10



90° phase shift fluctuations



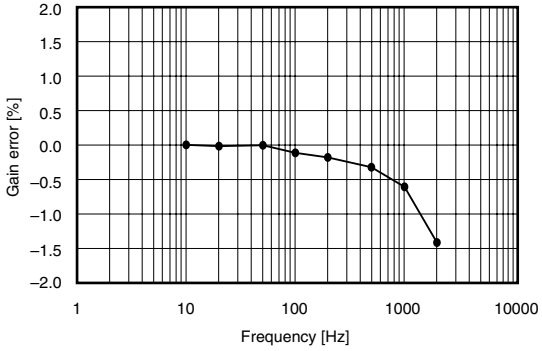
Phase offset



Characteristics CD-552R4

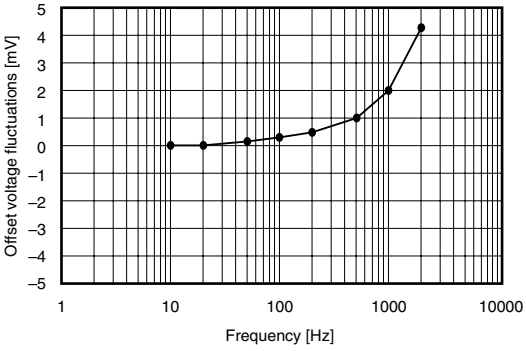
Gain fluctuations

Reference: 10kHz, Gain: ×10

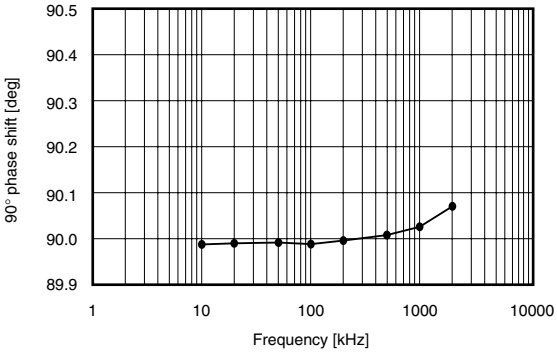


Offset voltage fluctuations

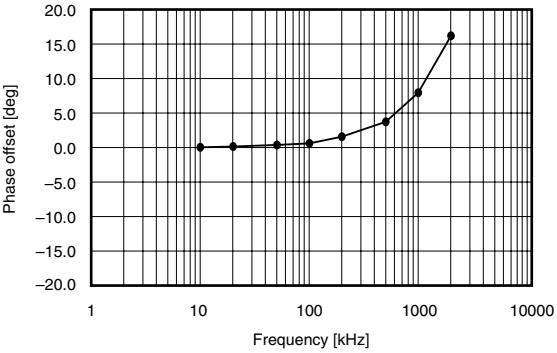
Reference: 10kHz, Gain: ×10



90° phase shift fluctuations

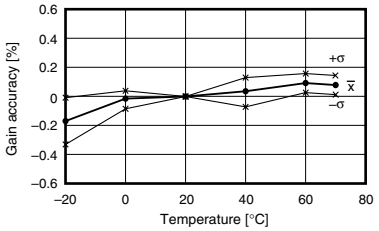


Phase offset

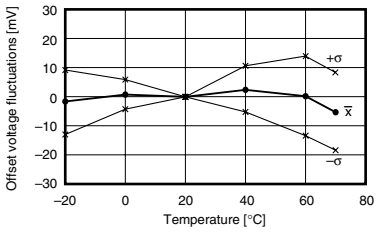


Characteristics CD-552R3

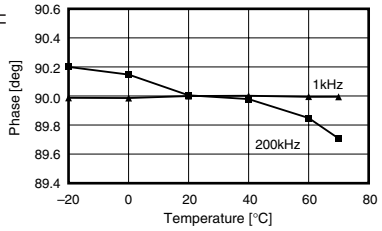
Gain accuracy – Temperature



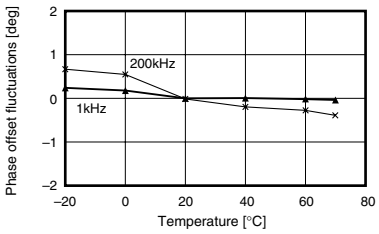
Offset voltage – Temperature



90° phase shift accuracy – Temperature

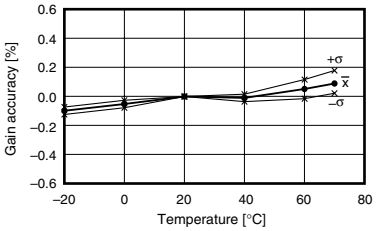


Phase offset – Temperature

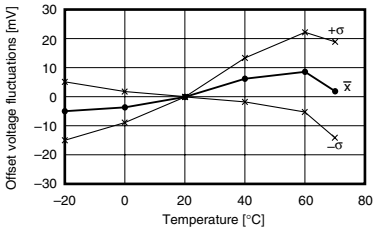


Characteristics CD-552R4

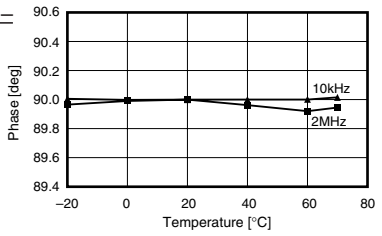
Gain accuracy – Temperature



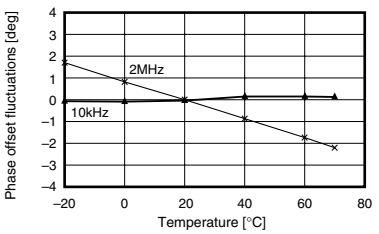
Offset voltage – Temperature



90° phase shift accuracy – Temperature

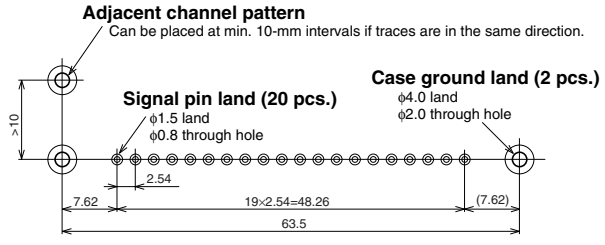


Phase offset – Temperature

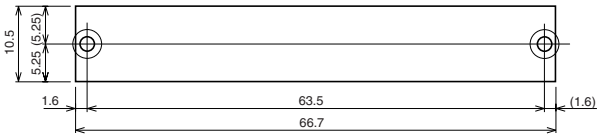


Pattern design

Proper connection between the case ground and the GND potential should always be assured. No sufficient shielding effect is produced if disregarded.
No signal traces should be assigned on the maximum visible outline of the component mounting surface. Possible contact between the metal case and the board is observed around the maximum visible outline, which triggers the establishment of a short circuit between the signal and case. A ground plane pattern is recommended to incorporate into the maximum visible outline and the inside of the case to enhance shielding effect.



Pattern dimensions



Maximum outer dimensions

To assure dynamic range and stability

■*Signal pre-processing*

If a sufficient S/N ratio fails to be obtained by the optimization of detector input level or setting of the output amplifier, a filter needs to be inserted in front of the detector to enhance the S/N ratio of input signal.
The filter falls into the four types (low-pass, high-pass, band pass, and band elimination) and becomes a determinant of the following items: asynchronous signal frequency component, amplitude characteristics, filter characteristics, and cut-off frequency.
The band pass filter attenuates all signals other than synchronization signal, which maximizes the improvement of the S/N ratio. Relatively large variations in phase around the center frequency, which may lead to detection accuracy if a phase change is made in response to temperature drift. Phase drift is minimized if low-order (1-pole if possible) Q is assigned.
The low-/high-pass filters attenuate low-/high-pass signals, and offer the smaller improvement of the S/N ratio as compared with the band pass filter. A phase change at a pass band is curbed, which contributes to a smaller detection accuracy attributed to fluctuations in cut-off frequency.
The band elimination provides large attenuation to signals of specified frequencies. An efficient improvement of the S/N ratio is obtained if specified frequency is assigned to the asynchronous signal. The least phase change at a pass band is assured, which minimizes a detection accuracy attributed to fluctuations in cut-off frequency.

■*Input signal level*

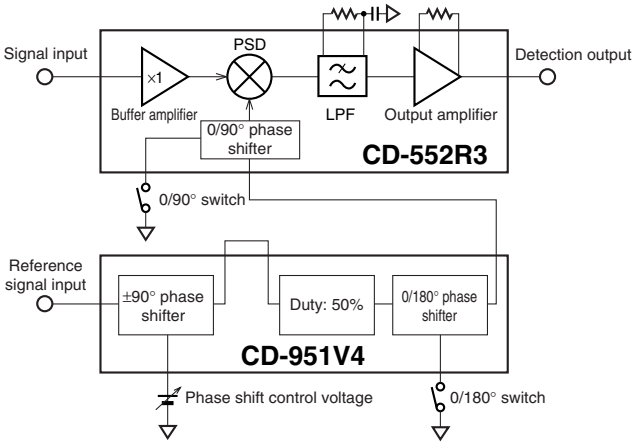
CD-552R3/4 detectors features $10V_{0}$-p of the maximum input level. A dynamic range can be assured if a large level of synchronization signal is input by maintaining within $10V_{0}$-p. The actual input signal contains both asynchronous and synchronization signals, which requires a decrease in the amplitude of $10V_{0}$-p or less.
E.g.: $0.1V_{0}$-p synchronization signal is present in $1V_{0}$-p signal that is a total of asynchronous and synchronization signals. CD-552R3/4 detectors performs the detection of the signals at 1Vdc of output despite the ×10-post-stage DC amplifier being designated. The allowable input level enables a ×10-amplifier to be inserted in front of the CD-552R3/4 detectors to input the maximum input voltage of $10V_{0}$-p. The detection output obtains 10Vdc when the ×10-post-stage DC amplifier is designated, which allows the obtainment of the maximum output signal.

■*Output amplifier*

The output amplifier is capitalized on to obtain a proper output level if a small detection output remains despite the optimization of input signals. CD-552R3/4 detectors are outfitted with the variable-gain output amplifiers (×1 to ×10). The maximum output voltage is set at $10V_{0}$-p that should not be surpassed when setting gain to assure proper voltage for post processor.
Note that an increase in DC drift, offset voltage and output noise is considered with an increase in gain.

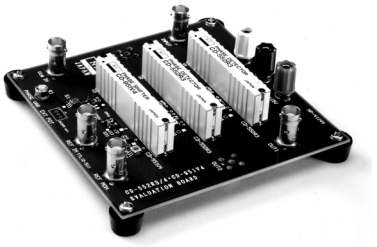
Phase adjustment

Phase detection with the use of the CD-552R3/4 detectors may require phase adjustment for the optimization of detection sensibility and cancellation of processing phase.
Phase adjustment is conducted in combination with the voltage controlled phase detector CD-951V4. Continuous change in phase shift of the reference signal is enabled through DC voltage.



Evaluation board

A module-mounted evaluation board is available for easy evaluation of this module. Contact us for further information.



Phase Shifter

CD-951V4

CD-951V4 is a 360°-voltage controlled phase shifter in the frequency range of 1kHz to 2MHz, and adopts CMOS-level (0/+5V) square wave for input and output. This is composed of the ±100°-variable voltage controlled phase circuit and 50%-duty circuit (PAT.P) with 0/180° switch. The combination use of the ±100°-phase shifter and 0/180°-selector enables the output of 50%-duty square wave that phase is shifted in the 360° range to the phase shifter input signal.
Double frequency is produced by the 50%-duty input signal if 2f mode is placed through the connection with the specified pin.
CD-951V4 is in a static-shielded 20-pin single-inline package, which is a great contributor to the implementation of high precision signal processing and high density mounting.

▼Absolute maximum ratings

Supply voltage (±Vs)	±18V
Phase control DC input voltage	±Vs
Phase shifter input voltage	+5.5V, –0.5V
Logic control voltage	+5.5V, –0.5V

▼50%-duty output/voltage control phase shifter

▽**Setting**

Setting	Pins ⑮-⑯ shorted, Pin ⑰ open
I/O characteristics	50%-duty square wave, which a phase is shifted by voltage control, is output with reference to the edge specified at polarity switch of phase shifter input signal waveform.

▼Frequency range

Frequency range	1kHz to 2MHz (2 ranges available: 1kHz to 200kHz, 10kHz to 2MHz)
Range switch	Pin ⑫ open or +5V: 1kHz to 200kHz 0V: 10kHz to 2MHz

▼Phase shifter input characteristics

Input circuit	CMOS Schmitt trigger, pulled up at 100 kΩ
Trip point	+3.5V/+1.5V (typ)
Input voltage	CMOS (0/+5V) level
Unipolar (1f) mode	A rising or falling edge is regarded as a reference.
Polarity switch	Pin ⑬ open or +5V: Rising edge regarded as a reference 0V: Falling edge regarded as a reference
Pulse duration	Min. 50ns
Bipolar(2f) mode	Both rising and falling edge are regarded as a reference.
Mode setting	Connected with the phase shifter input (Pin ⑭) and polarity switch input (Pin ⑬).
Input waveform	Duty : 50%
Input frequency range	1kHz to 1MHz

▼Voltage control characteristics

Control method	Phase shift is specified in the proportion to phase control DC input voltage.
Input resistance	100kΩ ±3% (DC)
Linear maximum input voltage	±5V (≤1MHz)
Linear control range	±90°
Voltage control sensitivity	–20°/V (–100°/+5V, 100°/–5V)
Sensitivity accuracy	±1°/V

▽**Phase shifter output characteristics**

Output circuit	HCMOS output, series resistor at 100Ω
Output voltage	CMOS (0/+5V) level
Duty	50%±0.03% (typ) (at 200kHz) 50%±0.3% (typ) (at 2MHz)
0/180° switch	Pin ⑳ open or +5V : –180°, 0V : 0°
–180° accuracy	–180°±0.02° (typ) (at 200kHz) –180°±0.2° (typ) (at 2MHz)
Phase offset	(1kHz to 200kHz) –0.6° (typ) (at 1kHz) –4.5° (typ) (at 200kHz) (10kHz to 2MHz) –0.9° (typ) (at 10kHz) –42.0° (typ) (at 2MHz)
Phase offset adjustment	Adjustment available with a 20kΩ-external potentiometer. (Pin ②)
Adjustment range	±5° (typ)

▼Reference voltage

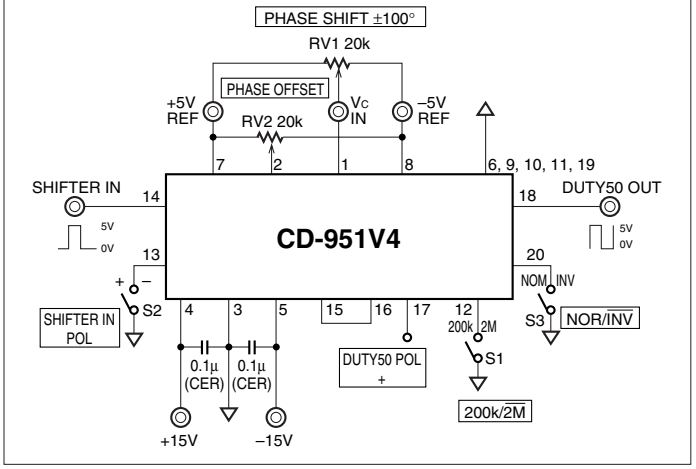
Output voltage/accuracy	Max. ±5V±2%
Temperature stability	50ppm/°C (typ)
Maximum output current	±1mA

▼Others

Recommended supply voltage		±15V±1V
Quiescent current		+25mA (max), +18mA (typ) –20mA (max), –12mA (typ)
Temperature/ humidity range	**Operation**	–20°C to 70°C, 10 to 90%RH
	Storage	–30°C to 80°C, 10 to 80%RH
Dimensions		67×10.5×20mm (protrusion not included) Type SS20 (20-pin shielded SIP)
Weight (NET)		Approx. 20g

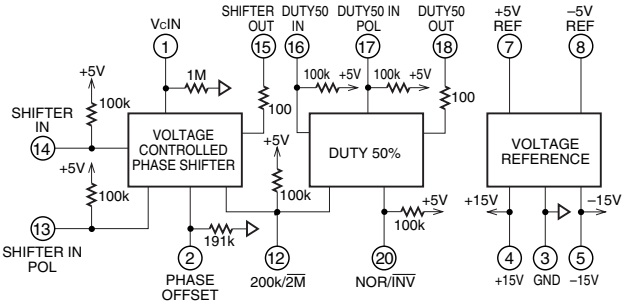
Note: The following specifications are applied unless otherwise specified:
23±5°C, Supply voltage: ±15V

Basic connection diagram



Phase Detectors

Block diagram



SHIFTER IN POL — This is used to switch the reference polarity of shifter input. The operation at double frequency, as compared with the reference signal, is actualized through the connection between the SHIFTER IN POL terminal and SHIFTER IN terminal if 50% of duty is assigned to the reference signal.

- HI: Rising edge regarded as a reference (specified when the pin is open)
- LO: Falling edge regarded as a reference

Connected with SHIFTER IN terminal:
Both rising and falling edge regarded as a reference

PHASE OFFSET — This is used to cancel phase offset. Zero adjustment of the phase offset for CD-951V4 phase shifter only is enabled in the range of 1kHz to 200kHz. Both terminals of a trimmer potentiometer of 20kΩ min. are connected with ±5V input (Pins ⑥ and ⑦), and the center terminal is connected to the PHASE OFFSET terminal.

200k/$\overline{2M}$ — This is used to switch the operating frequency range between 1kHz-200kHz and 10kHz-2MHz in response to the used frequency.

- HI: 1kHz to 200kHz (The pin is open)
- LO: 10kHz to 200MHz

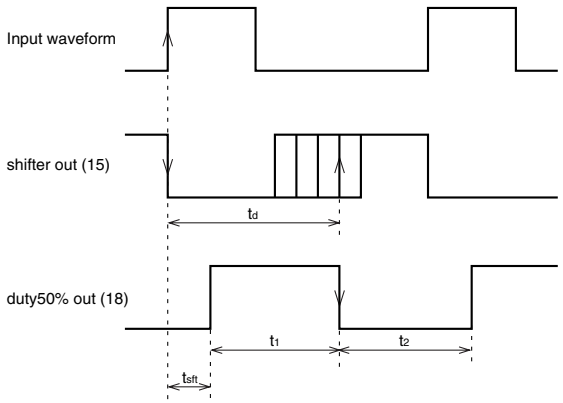
NOR/$\overline{INV}$ — This is used to switch the output phase between 0° and 180°. A 360°-phase shifter is configured in combination with a continuously variable phase shifter (±90°).

- HI: 0° (The pin is open)
- LO: 180°

DUTY50 IN POL — This is used to switch the input polarity of the 50%-duty circuit. "HI" (open) should remain on for normal connection.

- HI: Rising edge regarded as a reference (The pin is open)
- LO: Falling edge regarded as a reference

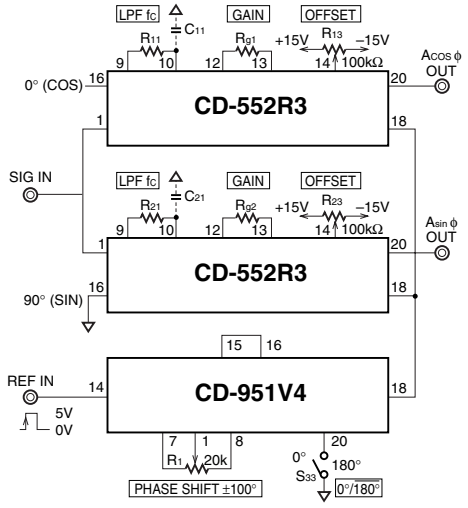
Timing chart



This timing chart presents the operation of the voltage controlled phase shifter CD-951V4.
E.g.: The CD-951V4 phase shifter is set to regard a rising edge of the input signal as a phase reference. This detector produces the signal "LO" (Pin ⑮) for the time proportionate to the control voltage (td) if a rise is observed in the input signal (Pin ⑭).
Waveform shaping (Pin ⑱) is performed to assure 50% in duty (t1 = t2) with reference the rising edge in the obtained signal.
td adjustment allows continuous change in input/output rise time (tsft), which denotes phase change.
The same operating principles* are applied to the phase detector CD-552R3 that has realized 90°-phase shift with high accuracy.

* Patent pending

Usage example 2-phase detector



This example indicates the adoption of this detector to the 2-phase detector. The cos and sin detection outputs are obtained, which allows amplitude and phase of the synchronization signals to be derived from the relevant vector operation.
The settings of GAIN (×1 to ×10) and LPFfc (max. 1kHz) are available in this detector. Offset adjustment is required as necessary.
Phase adjustment is available by 90°-continuous phase shift (CD-951V4 R1) or 0/180°-switch (S33), which enables 360°-phase change in total.

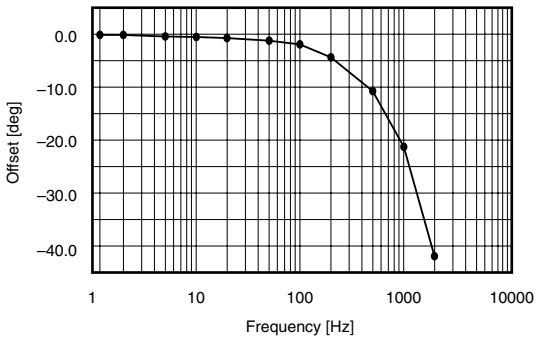
GAIN setting: Short: ×10
Open: ×1

LPFfc setting (same as R21):
Short: 1kHz

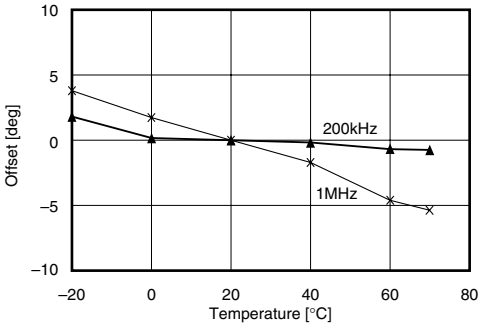
Note: See the CD-552R3/R4 in Page 72 for details in the GAIN setting and LPF setting.

Characteristics

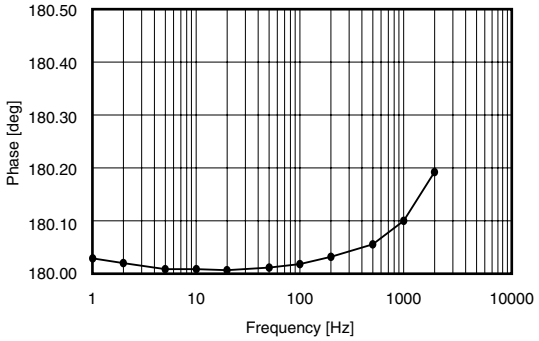
Phase offset



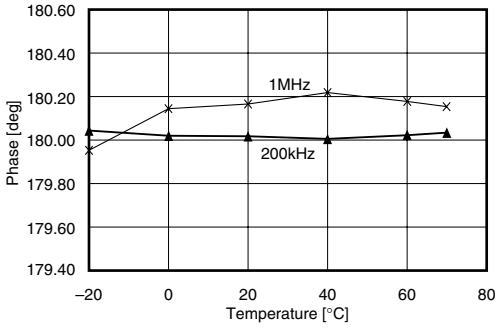
Phase offset - Temperature



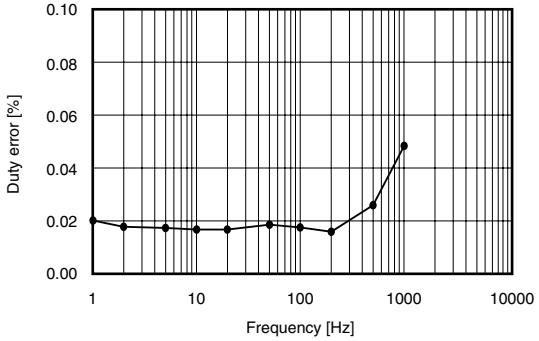
180° phase error



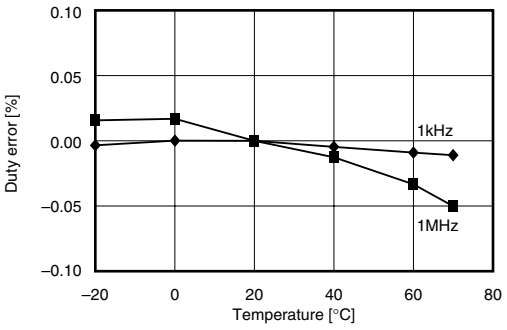
180° phase error - Temperature



Duty error



Duty error - Temperature



Control voltage coefficient – Temperature